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09/834,954	04/16/2001	Tomohide Terashima	57454-062	5366

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EXAMINER

MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 01/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/834,954

Applicant(s)

TERASHIMA, TOMOHIDE

Examiner

Johannes P Mondt

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04/16/01.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement filed 04/16/01 entered as Paper No. 4.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. *Claims 2, 3, and 11 are rejected* under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, in *claims 2 and 11* the electrode part is claimed to be sandwiched between said third impurity region and said semiconductor layer; however, all electrode parts shown in all of Applicant's figures are on the upper side of all semiconductor regions and layers, as is standard in the art, and thus it is rendered unclear as to how to use the invention as stipulated by claim 2. *Claim 3* depends on claim 2 and therefore also is rejected herewith.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. *Claims 1 and 5 are rejected* under 35 U.S.C. 103(a) as being unpatentable over Galbiati et al (5,629,558) in view of Ludikhuize (IEEE publication).

With regard to claim 1:

Galbiati et al teach a semiconductor device including:

a semiconductor substrate 2 (cf. column 2, lines 18-20) having a main surface (cf. Fig. 1);

a semiconductor layer 9 (cf. column 2, lines 54-57) of first conductivity type (N type) formed on the main surface of said semiconductor substrate (cf. Fig. 1);

a first buried impurity region 3 of first conductivity type (N type) (cf. column 2, lines 20-23) formed between said semiconductor layer and said semiconductor substrate (note that 9 and 6 are part of the same original epitaxial layer) (cf. Fig. 1);

a second buried impurity region 4 of second conductivity type (P type) (cf. column 2, lines 24-26) formed between said first buried impurity region and said semiconductor layer (cf. Fig. 1);

a first impurity region 10 (cf. column 2, line 56) of second conductivity type (P type) formed in the surface of said semiconductor layer and contacting said second buried impurity region while having the same conductivity type as said

second buried impurity region, and thus electrically connected to said second buried impurity region (cf. Fig. 1);

a second, highly doped, impurity region 14, of the first conductivity type (N type) (cf. column 2, lines 49-53) which is formed in the surface (or inside) of said semiconductor layer located in a region above said second buried impurity region;

a semiconductor element, namely diode 1 (cf. column 2, lines 15-18), formed on the surface of the aforementioned semiconductor layer, and which semiconductor element includes said impurity region,

wherein the withstanding voltage is secured by a depletion layer extending from an interface between said impurity region and said semiconductor layer under the condition where (when) said semiconductor element is turned OFF (cf. column 2, lines 60-67); and

said second buried impurity region 4 includes recessed parts (plural; which is relevant to claim 5; see below) called 'depressions' (cf. column 2, lines 31-35) wherein a surface of said buried impurity region is recessed in the direction away from said second impurity region 4 in part(s) 5 located, approximately, directly beneath a first gap part(s) where said second buried impurity region is disconnected (cf. Fig. 1).

Galbiati et al do not specifically teach the semiconductor element to have a switching function.

However, it belongs to the standard applications of diodes to be used for the purpose of switching, as shown, among numerous papers and patents for instance by the publication by Ludikhuize. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the stipulation that the semiconductor element of claim 1 has a switching function.

With regard to claim 5: said second buried impurity region as taught by *Galbiati et al* has a plurality of said first recessed parts, namely two first recessed parts 5 (cf. Fig. 1), hence claim 5 does not distinguish over the prior art.

3. *Claims 4 and 9 are rejected* under 35 U.S.C. 103(a) as being unpatentable over *Galbiati et al* and *Ludikhuize* as applied to claim 1 above, and further in view of *Terashima* (5,874,767).

With regard to claim 4: as detailed above, claim 1 is unpatentable over *Galbiati et al* in view of *Ludikhuize*, who do not necessarily teach an additional third (N.B.: not 'fifth' as stated erroneously in claim 4: there are only two impurity regions in claim 1) impurity region of the second conductivity type formed on a surface of said semiconductor layer. However, as taught in a previous U.S. patent (No. 5,874,767) by Applicant *Terashima*, for the purpose of isolation the second impurity region (of first conductivity type) can be surrounded by an additional impurity region of opposite conductivity type, here second conductivity or P type (cf. column 14, lines 30-33 of claim 6). Therefore, it would have

been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the further limitation of claim 4.

With regard to claim 9: the junction interface between said first buried impurity region 3 and said second buried impurity region 4 as taught by Galbiati et al is indeed uneven (cf. Fig. 1). Therefore, the further limitation of claim 9 does not distinguish over the prior art.

4. *Claims 6-8 are rejected* under 35 U.S.C. 103(a) as being unpatentable over Galbiati et al and Ludikhuize as applied to claims 1 and 5 above, and further in view of Singer (4,485,392).

With regard to claim 6: as detailed above, claims 1 and 5 are unpatentable over Galbiati et al in view of Ludikhuize, who do not necessarily teach the semiconductor device wherein said second buried impurity region includes a plurality of first gap parts. However, in view of Singer, who teaches gaps 14A on both sides of portion 13B of the buried impurity region 13A/13B for the purpose of enabling the selection of a proper cut-off voltage (cf. column 5, lines 37-49 and 50-63; also, cf. Fig. 4), a modification of the semiconductor device of claim 5 consisting of the replacement of said plurality of said first recessed parts 5 by gaps should have been obvious to one of ordinary skills in the art at the time the invention was made, particularly since the tendencies of recessed parts and gaps are obviously the same, the latter being extrapolations of the former.

With regard to claim 7: the buried impurity region taught by Singer features a plurality of gaps, i.e., at least two, located on the left and right hand sides of 13B, by

virtue of which said buried impurity region includes a plurality of regions, i.e., buried layer portions 13A and 13B (cf. column 4, lines 53-54); it is inherent to their electrical environment that said regions are electrically floating, because of the absence of any connection with a good conductor that would maintain a certain electrostatic potential within them.

With regard to claim 8: neither Galbiati et al, nor Ludikhuize nor Singer specifically teach the surface of the first buried impurity region to be recessed away from said second buried impurity region in a location approximately beneath said first gap part or a second gap part wherein said first buried impurity region is disconnected. However, such recess away would be of obvious advantage since the effective thickness of the epitaxial layer would thereby be increased, resulting in a corresponding increase in breakdown voltage, which is the basis of the invention by Galbiati et al (cf. abstract and column 1, lines 48-58). It thus would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to stipulate the further limitation of claim 8.

5. *Claims 10, 12, and 13 are rejected* under 35 U.S.C. 103(a) as being unpatentable over Galbiati et al (5,629,558) in view of Ludikhuize (IEEE publication), Singer (4,482,392), and Harris et al (6,127,695).

With regard to claim 10: as detailed above in the discussion of claim 1, Galbiati et al teach all aspects of claim 10 except for the stipulation that the semiconductor element be used for performing switching functions and for the presence of the first buried

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impurity region 3 in Gabliati et al underneath the second buried impurity region 4 while in the present claim 10 said first buried impurity region 3 is absent. However, in a lateral junction field effect device such as the one taught by Singer there is no need for region 3 (see Fig. 2), while, as has already been discussed in connexion with claim 6, Singer who teaches gaps 14A on both sides of portion 13B of the buried impurity region 13A/13B for the purpose of enabling the selection of a proper cut-off voltage (cf. column 5, lines 37-49 and 50-63; also, cf. Fig. 4). Because the function of the gaps and recessed parts are identical in that the breakdown voltage is increased through an effective increase in the available layer immediately below the gate it would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made to incorporate the embodiment suggested by Singer, in which all of the invention by Gabliati et al, with the possible exception of the required switching function of the semiconductor element, can be carried over with the sole proviso that the buried impurity region 3 can be dispensed with. Finally, that lateral field effect transistors are widely known to be useful for the performance of switching function is shown for instance by Harris et al (cf. title and abstract, first sentence).

With regard to claim 12: in addition to impurity regions 10 and 14 mentioned above, Gabliati et al teach impurity region 13, while, parenthetically both regions 13 and 14 are clearly depicted to consist of two impurity regions (cf. Fig. 1). Therefore, the further limitation of claim 12 does not distinguish over the prior art.

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With regard to claim 13: inherently, the depletion layer extends below the gate area, which is where the gap is formed in the invention of Singer (cf. column 5, lines 55-63). Therefore, the further limitation of claim 13 does not distinguish over the prior art.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gabliati et al (5,940,700).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
January 7, 2002

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